NISIN

内嵌式触摸液晶显示模组规格承认书

(IN-CELL)LCM Specifications for Approval

客户： 客户型号：			NS650FH4004AZ01		
批准 APPROVED	审核 CHECKED	拟制 DESIGNED	批准 APPROVED	审核 CHECKED	拟制 DESIGNED

修改记录

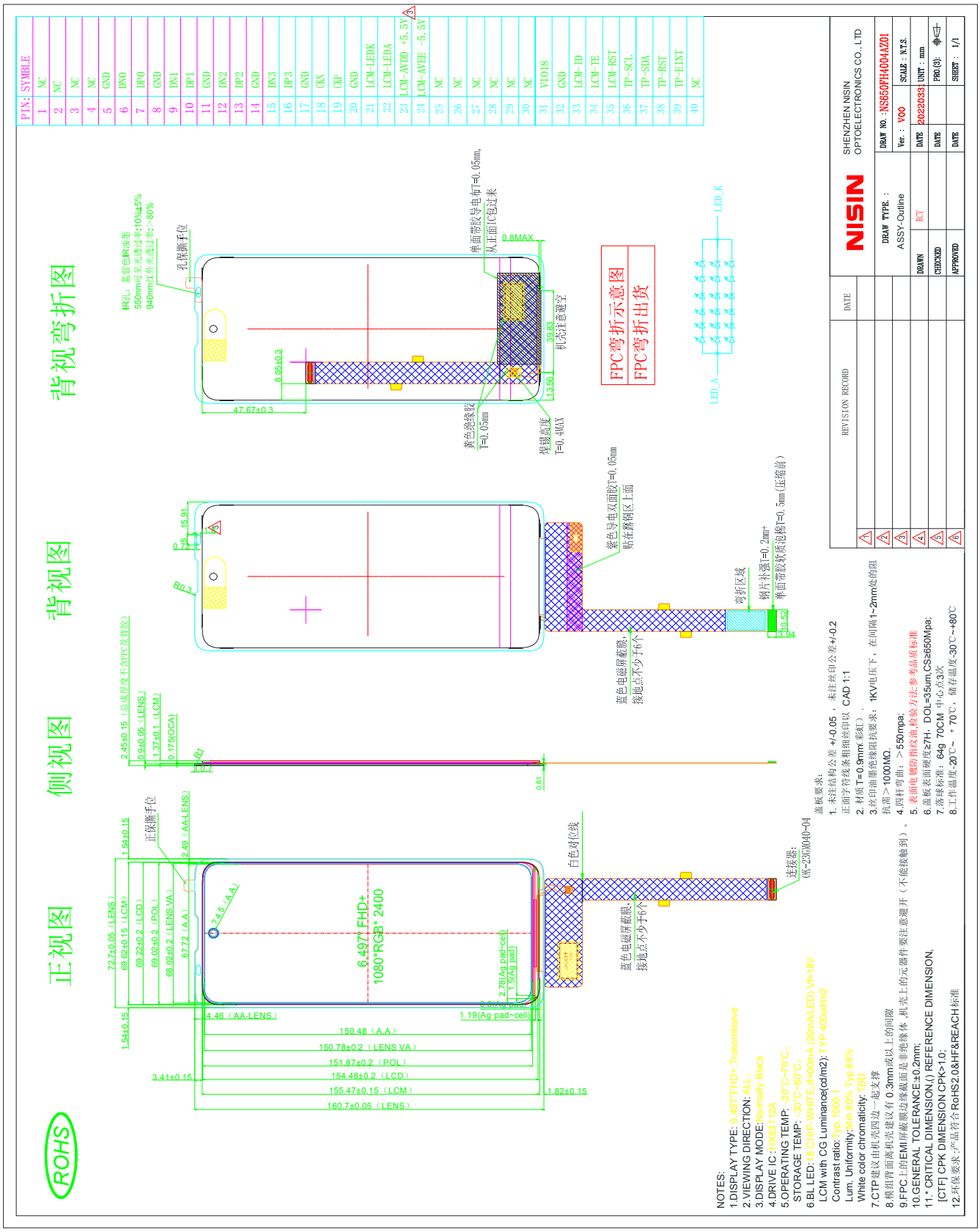
日期	版本	修改内容	页数	拟制
2022-5-26	V00	初版发行	所有	

目录

1.产品规格（Product Specifications）

面板类型（Panel Type）	a-si TFT
面板尺寸(Panel Size)	6.5 inch
显示类型（Display Type）	Normal Black
分辨率（Resolution）	1080(RGB) x 2400 (dot)
显示点间距（Dot Pitch）	0.0209mm X 0.0627mm
显示色彩（color）	16.7M
视角（View Angle）	ALL
显示驱动 IC（Display Driver IC）	HX83112A
接口类型（Interface Type）	MIPI 4 Lane
触摸类弄（TP Type）	INCELL
触摸 IC （TP IC）	HX83112A
触摸接口类型（TP Interface）	I2C
外形尺寸（Dimensions）	72.7(H) X 160.7(V) X 2.45(T) (mm)
显示区尺寸（Display area）	67.72 x 150.48(mm)
背光（Back Light）	590 Cd/m^2 （TYP）
触摸点数 Touch points	5
触摸按键 Touch Key Number	0

2. 产品图纸（Product Drawings）



3.接口定义（The Interface Definition）

见 CAD 图纸

4.电性特性（Electrical Characteristics）

7.1 Absolute maximum ratings

The absolute maximum ratings are list on Table 7.1. When used out of the absolute maximum ratings, the LSI may be permanently damaged. Using the LSI within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the LSI will malfunction and cause poor reliability.

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Power supply voltage 1(1),(2)	VDD1~ VSSD	-0.3	-	+7.5	V
Power supply voltage 2(3)	VSP ~ VSSA	-0.3	-	+7.5	V
Power supply voltage 3(4)	VSSA ~ VSN	0	-	-7.5	V
Power supply voltage 4(5)	VGH ~ VSSA	-0.3	-	+16	V
Power supply voltage 5(6)	VSSA ~ VGL	-15	-	0	V
Power supply voltage 6(7)	VGHO ~ VSSA	-0.3	-	+15.6	V
Power supply voltage 7(8)	VSSA ~ VGLO	-13.6	-	0	V
Operating temperature(9)	T_A	-40	-	+85	°C
Storage temperature(10)	Tstg	-55	-	+110	°C
Input voltage(11)	V_{IN}	-0.3	-	VDD1+0.3	V
HS input voltage(12)	V_{HSIN}	-0.3	-	+2	V

Note: (1) VDD1, VSSD must be maintained.
(2) To make sure VDD1 ≥ VSSD.
(3) To make sure VSP ≥ VSSA.
(4) To make sure VSSA ≥ VSN
(5) To make sure VGH ≥ VSSA.
(6) To make sure VSSA ≥ VGL, VGH +|VGL| < 32V.
(7) To make sure VGHO ≥ VSSA.
(8) To make sure VSSA ≥ VGLO
(9) For die and wafer products, specified up to +85°C.
(10) This temperature specifications apply to the TCP package.
(11) This specifications include input signals but without following: CP, CN, D0P, D0N, D1P, D1N, D2P, D2N, D3P, D3N.
(12) This specifications include following signals: CP, CN, D0P, D0N, D1P, D1N, D2P, D2N, D3P, D3N.

Table 7.1: Absolute maximum rating

7.2 DC characteristics

(VDD1=1.8V, T_A= 25 °C)

Parameter	Symbol	Test condition	Spec.			Unit
			Min.	Typ.	Max.	
Input high voltage	V_{IH}	VDD1= 1.65 ~ 1.95V	0.7VDD1	-	VDD1	V
Input low voltage	V_{IL}		0	-	0.3VDD1	V
Output high voltage	V_{OH1}	I_{OH} = -1.0 Ma	0.8VDD1	-	-	V
Output low voltage	V_{OL1}	VDD1= 1.65 ~ 1.95V I_{OL} = 1.0 mA	0	-	0.2VDD1	V
Logic High level input current	I_{IH}	RESX, DCX, RDX, CSX, SCL_WRX, SDI_SDA	-	-	1	µA
Logic Low level input current	I_{IL}	RESX, DCX, RDX, CSX, SCL_WRX, SDI_SDA	-1	-	-	µA
Current consumption SLP IN mode **(VDD1 - VSSD)**	$I_{ST(VDD1)}$	VDD1=1.8V VSP=5.5V VSN=5.5V T_A =25°C Touch idle mode	-	800	1600	µA
Current consumption SLP IN mode **(VSP - VSSA)**	$I_{ST(VSP)}$		-	45	160	µA
Current consumption SLP IN mode **(VSSA - VSN)**	$I_{ST(VSN)}$		-	20	80	µA
Current consumption Deep Standby mode **(VDD1 - VSSD)**	$I_{ULPS(VDD1)}$	VDD1=1.8V VSP=0V VSN=0V T_A =25°C	-	25	70	µA
Current consumption Deep Standby mode **(VSP - VSSA)**	$I_{ULPS(VSP)}$		-	0	-	µA
Current consumption Deep Standby mode **(VSSA - VSN)**	$I_{ULPS(VSN)}$		-	0	-	µA
Oscillator tolerance(1)	Δ OSC	T_A =25°C	-2	-	2	%

Note: (1) Oscillator tolerance with auto tracking.

Table 7.2: DC characteristics

7.3 AC characteristics

7.3.1 DSI D-PHY electrical characteristics

7.3.1.1 Electrical characteristics of D-PHY layer

In general, the DSI D-PHY may contain the following electrical functions: High-Speed Receiver (HS-RX), Low Power Transmitter (LP-TX), a Low-Power Receiver (LP-RX), and the Low-Power Contention Detector (LP-CD). Figure 7.1 shows the complete set of electrical functions required for a fully featured PHY transceiver.

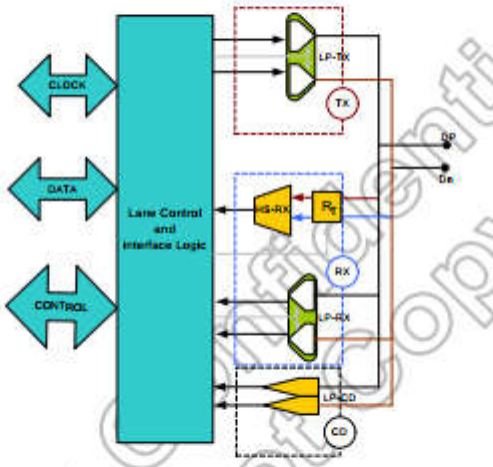


Figure 7.1: Electrical functions of a fully D-PHY transceiver

Where, the HS receiver utilize low-voltage swing differential signaling for signal transmission. The LP transmitter and LP receiver serve as a low power signaling mechanism. Figure 7.2 shows both the HS and LP signal levels on the left and right sides, respectively.

Because the HS signaling levels are below the LP low-level input threshold, Lane switches between Low-Power and High-Speed mode during normal operation.

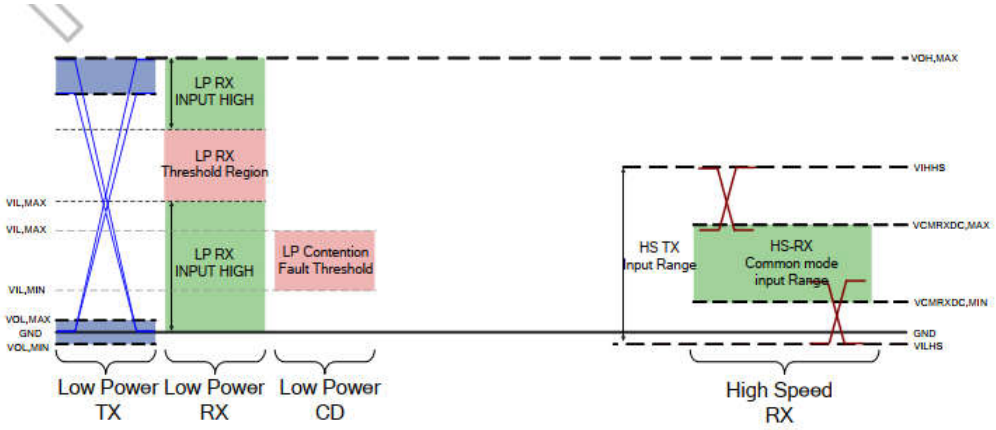


Figure 7.2: Shows both the HS and LP signal levels

7.3.1.2 Electrical characteristics of low-power transmitter

The Low-Power transmitter shall be a slew-rate controlled push-pull driver. It is used for driving the Lines in all Low-Power operating modes It is therefore important that the static power consumption of a LP transmitter be as low as possible. Under tables list DC and AC characteristic for LP-TX.

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Thevenin output low level	V_{OL}	-50	-	50	mV
Thevenin output high level	V_{OH}	1.1	1.2	1.3	V
Output impedance of LP-TX(1)	Z_{OLP}	110	-	-	Ω

Note: (1) Though no maximum value for Z_{OLP} is specified, the LP transmitter output impedance shall ensure the t_{RLP}/t_{FLP} specification is met.

Table 7.3: LP transmitter DC specifications

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
15%-85% rise time and fall time(1)	t_{RLP}/t_{FLP}	-	-	25	ns
Slew rate @ C_{LOAD} =0pF(1),(2),(3),(4)	$\delta V/\delta t_{SR}$	-	-	500	mV/ns
Slew rate @ C_{LOAD}=5pF(1),(2),(3),(4)		-	-	300	mV/ns
Slew rate @ C_{LOAD}=20pF(1),(2),(3),(4)		-	-	250	mV/ns
Slew rate @ C_{LOAD}=70pF(1),(2),(3),(4)		-	-	150	mV/ns
Slew rate @ C_{LOAD}=0 to 70pF(1),(2),(5) **(Falling edge only)**		30	-	-	mV/ns
Slew rate @ C_{LOAD}=0 to 70pF(1),(2),(6) **(Rising edge only)**		30	-	-	mV/ns
Slew rate @ C_{LOAD}=0 to 70pF(1),(7),(8) **(Rising edge only)**		30 – 0.075 * (VO,INST- 700)	-	-	mV/ns
Load capacitance	C_{LOAD}	-	-	70	pF

Note: (1) C_{LOAD} includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay.
(2) Measured as average across any 50 mV segment of the output signal transition.
(3) This value represents a corner point in a piecewise linear curve.
(4) When the output voltage is in the range specified by VPIN **(Absmax)**.
(5) When the output voltage is between 400 mV and 930 mV.
(6) When the output voltage is between 400 mV and 700 mV.
(7) Where VO,INST is the instantaneous output voltage, VDP or VDN, in millivolts.
(8) When the output voltage is between 700 mV and 930 mV.

7.3.1.3 Electrical characteristics of receiver

There part will contain two parts which High-Speed Receiver and Low-Power Receiver. Because their have differential DC and AC characteristic, describe HS-RX first then describe LP-RX.

7.3.1.4 High-speed receiver

The HS receiver is a differential line receiver. It contains a switch-able parallel input termination, Z_{ID}, between the positive input pin Dp and the negative input pin Dn. Under Tables list DC and AC characteristic for HS-RX.

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Differential input high threshold	V_{IDTH}	-	-	70	mV
Differential input low threshold	V_{IDTL}	-70	-	-	mV
Single-ended input low voltage(1)	V_{ILHS}	-40	-	-	mV
Single-ended input high voltage(1)	V_{IHHS}	-	-	460	mV
Common-mode voltage HS receive mode(1),(2)	V_{CMRXDC}	70	-	330	mV
Differential input impedance	Z_{ID}	80	100	125	Ω

Note: (1) Excluding possible additional RF interference of 100mV peak sine wave beyond 450MHz.
(2) This table value includes a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450MHz

Table 7.5: HS receiver DC specifications

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Common mode interference beyond 450 MHz(1)	$\Delta V_{CMRX(HF)}$	-	-	100	mV_{PP}
Common mode termination(2)	C_{CM}	-	-	60	pF

Note: (1) $\Delta V_{CMRX(HF)}$ is the peak amplitude of a sine wave superimposed on the receiver inputs.
(2) For higher bit rates a 14pF capacitor will be needed to meet the common-mode return loss specification.

Table 7.6: HS receiver AC Specifications

7.3.1.5 Low-power receiver

The low power receiver is an un-terminated, single-ended receiver circuit. The LP receiver is used to detect the Low-Power state on each pin. For high robustness, the LP receiver shall filter out noise pulses and RF interference. It is recommended the implementer optimize the LP receiver design for low power. The LP receiver shall reject any input glitch when the glitch is smaller than eSpike. The filter shall allow pulses wider than TMIN to propagate through the LP receiver. The related diagram shows as Figure 7.3 Input Glitch Rejection of Low-Power Receivers. Besides, under tables list DC and AC characteristic for LP-RX.

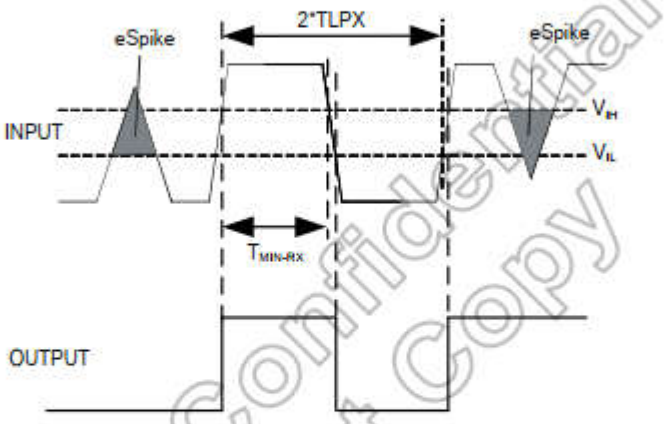


Figure 7.3: Input glitch rejections of low-power receivers

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Logic 0 input threshold	V_{IL}	-	-	550	mV
Logic 1 input threshold	V_{IH}	880	-	-	mV

Table 7.7: LP receiver DC specifications

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Input pulse rejection[1][2][3]	e_{SPIKE}	-	-	300	V.ps
Minimum pulse width response[4]	T_{MIN-RX}	20	-	-	ns
Peak-to-peak interference voltage	V_{INT}	-	-	200	mV
Interference frequency	f_{INT}	450	-	-	MHz

Note: (1) Time-voltage integration of a spike above VIL when being in LP-0 state or below VIH when being in LP-1 state.
(2) An impulse less than this will not change the receiver state.
(3) In addition to the required glitch rejection, implementers shall ensure rejection of known RF-interferers.
(4) An input pulse greater than this shall toggle the output.

Table 7.8: LP receiver AC specifications

7.3.1.6 Line contention detection

Contention can be inferred from any of the following conditions:

A. An LP high fault shall be detected when the LP transmitter is driving high and the pin voltage is less than V_{IHCD}.
B. An LP low fault shall be detected when the LP transmitter is driving low and the pad pin voltage is greater than V_{ILCD}.

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Logic 1 contention threshold	V_{IHCD}	450	-	-	mV
Logic 0 contention threshold	V_{ILCD}	-	-	200	mV

Table 7.9: Contention detector DC specifications

7.3.1.7 High-speed data-clock timing

This section specifies the required timings on the high-speed signaling interface independent of the electrical characteristics of the signal. The PHY is a source synchronous interface in the Forward direction.

The Master side of the Link shall send a differential clock signal to the Slave side to be used for data sampling. This signal shall be a DDR **(half-rate)** clock and shall have one transition per data bit time. All timing relationships required for correct data sampling are defined relative to the clock transitions. Therefore, implementations may use frequency spreading modulation on the clock to reduce EMI.

The DDR clock signal shall maintain a quadrature phase relationship to the data signal. Data shall be sampled on both the rising and falling edges of the Clock signal. The term "rising edge" means "rising edge of the differential signal, i.e. CP – CN, and similarly for "falling edge". Therefore, the period of the Clock signal shall be the sum of two successive instantaneous data bit times. This relationship is shown in Figure 7.4.

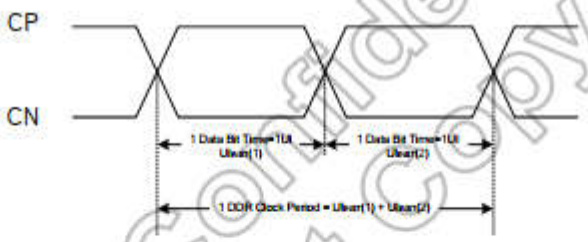


Figure 7.4: DDR clock definition

The same clock source is used to generate the DDR Clock and launch the serial data. Since the Clock and Data signals propagate together over a channel of specified skew, the Clock may be used directly to sample the Data lines in the receiver. Such a system can accommodate large instantaneous variations in UI.

The allowed instantaneous UI variation can cause large, instantaneous data rate variations. Therefore, devices shall either accommodate these instantaneous variations with appropriate FIFO logic outside of the PHY or provide an accurate clock source to the Lane Module to eliminate these instantaneous variations.

The UI_{INST} specifications for the Clock signal are summarized in Table 7.10.

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
UI instantaneous(1), (2), (3)	UI_{INST}	0.83	-	12.5	ns

Note: (1) This value corresponds to a minimum 80 Mbps/lane data rate.
(2) The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst.
(3) Maximum total bit rate is 4.8Gbps of at 24-bit data format /3.6Gbps at 18-bit data format / 3.2Gbps at 16-bit data format.

Table 7.10: Reverse HS data transmission timing parameters

The timing relationship of the DDR Clock differential signal to the Data differential signal is shown in Figure 7.5. Data is launched in a quadrature relationship to the clock such that the Clock signal edge may be used directly by the receiver to sample the received data.

The transmitter shall ensure that a rising edge of the DDR clock is sent during the first payload bit of a transmission burst such that the first payload bit can be sampled by the receiver on the rising clock edge, the second bit can be sampled on the falling edge, and all following bits can be sampled on alternating rising and falling edges.

All timing values are measured with respect to the actual observed crossing of the Clock differential signal. The effects due to variations in this level are included in the clock to data timing budget.

Receiver input offset and threshold effects shall be accounted as part of the receiver setup and hold parameters.

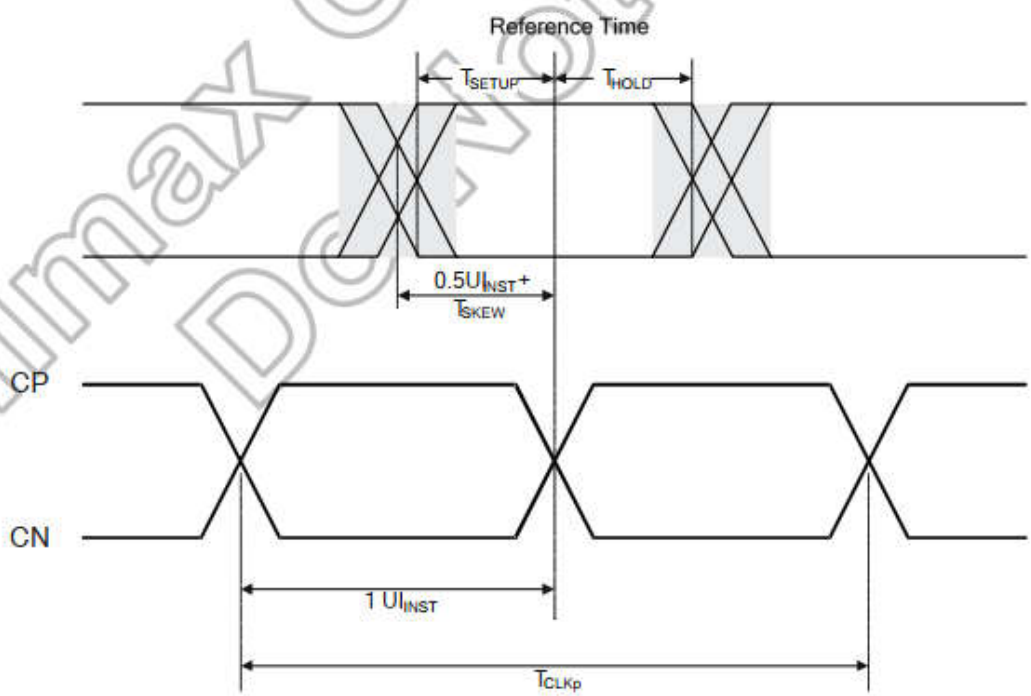


Figure 7.5: Data to clock timing definitions

7.3.1.8 Data-clock timing specifications

The Data-Clock timing specifications are shown in Table 7.11. Implementers shall specify a value UI_{INST}**(Min.)** that represents the minimum instantaneous UI possible within a High-Speed data transfer for a given implementation. Parameters in Table 7.11 are specified as a part of this value. The skew specification, $T_{SKEW[TX]}$, is the allowed deviation of the data launch time to the ideal ½UI_{INST} displaced quadrature clock edge. The setup and hold times, $T_{SETUP[RX]}$ and $T_{HOLD[RX]}$, respectively, describe the timing relationships between the data and clock signals. $T_{SETUP[RX]}$ is the minimum time that data shall be present before a rising or falling clock edge and $T_{HOLD[RX]}$ is the minimum time that data shall remain in its current state after a rising or falling clock edge. The timing budget specifications for a receiver shall represent the minimum variations observable at the receiver for which the receiver will operate at the maximum specified acceptable bit error rate.

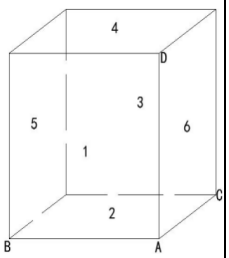
The intent in the timing budget is to leave 0.4*U_{IINST}, i.e. ±0.2*UI_{INST} for degradation contributed by the interconnect.

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Data to clock setup time [Receiver](1)	$T_{SETUP[RX]}$	0.15	-	0.85	UI_{INST}
Clock to data hold time [Receiver](1)	$T_{HOLD[RX]}$	0.15	-	0.85	UI_{INST}

Note: (1) Total setup and hold window for receiver of 0.3*UI_{INST}.

Table 7.11: Data to clock timing specifications

5.可靠性实验测试(Reliability Test Conditions And Methods)

<table>
<tr><th>序号</th><th>试验项目</th><th>试验条件及方法</th><th>试验设备</th><th>检验项目</th><th>检验工具</th></tr>
<tr><td>1</td><td>高温高湿(静、动态)试验</td><td>温度 60℃±3℃,湿度 90%±3%,要求选择时间分别为 96 小时,静、动态（产品点亮）在室温下恢复 2 小时后进行外观,显示功能检查。</td><td>恒温恒湿试验机</td><td>检验外观、功能、抗腐蚀性</td><td rowspan="2">目视/测试架/客户样机/显微镜</td></tr>
<tr><td>2</td><td>高、低温冲击试验</td><td>静态-30℃（30 分钟）∽ 80℃（30 分钟）∽ -30℃（30 分钟），24 个循环，在室温下恢复 2 小时后进行外观,显示功能检查。</td><td>冷热冲击试验机</td><td>检验外观、功能</td></tr>
<tr><td>3</td><td>高温存贮试验</td><td>常温60℃+-3℃、宽温70℃+/-3℃、96小时后在室温状态下恢复1 小时在2 小时内完成外观、显示功能检查。</td><td>烤箱</td><td>检验外观、功能</td><td rowspan="2">目视/测试架/客户样机</td></tr>
<tr><td>4</td><td>低温存贮试验</td><td>常温-20℃+/-3℃、宽温-30℃+/-3℃、条件的试验箱内保存96 小时后在室温状态下恢复1 小时,在2 小时完成外观、显示功能检查，特别注意检查是否有漏液、断线、腐蚀、偏光片不良现象。</td><td>低温冰箱</td><td>检验外观、功能</td></tr>
<tr><td>5</td><td>低温存贮试验（动态）</td><td>常温-20℃+/-3℃、宽温-30℃+/-3℃条件的试验箱内点亮刷屏，过程中每1小时观察一次，检查显示功能，如：异常，卡机，花屏等。特别注意检查是否有漏液、断线、腐蚀、偏光片不良现象。</td><td>低温冰箱</td><td>检验外观、功能</td><td>目视/测试架/客户样机</td></tr>
<tr><td>6</td><td>包装模组跌落试验</td><td>1、跌落重量及自由落体高度:（图二）
 

2、自由落体角度如下：
<table>
<tr><th>总重量</th><th>自由落体高度</th></tr>
<tr><td>0-9kg</td><td>92cm</td></tr>
<tr><td>9-25kg</td><td>76cm</td></tr>
<tr><td>25-45kg</td><td>53cm</td></tr>
<tr><td>45-68kg</td><td>46cm</td></tr>
<tr><td>大于 68kg</td><td>41cm</td></tr>
<tr><td></td><td></td></tr>
</table>
1） 一角：A角
2） 三菱：A-B, A-D, A-C
3） 六面：面 1，面 2，面 3，面 4，面 5，面 6;</td><td>包装模组跌落架</td><td>测试电性能无异常、外观检验无破损，无脱离现象</td><td>目视/测试架/客户样机</td></tr>
</table>

7	盐雾试验	标准条件:中性盐雾试验（NSS 试验）：5%的氯化钠盐水溶液,溶液 PH 值中性（6.5～7.2），试验温度 35±2℃,盐雾的沉降率在 1～2ml/80cm².h 之间,时间 24h。2.其它特殊要求条件:醋酸盐雾试验(ASS 试验)：5%氯化钠溶液中配入冰醋酸,溶液 PH 值为 3 左右，试验温度 35±2℃,盐雾的沉降率在 1～2ml/80cm².h 之间，时间 24h。	盐雾试验设备	检验外观、功能，盐雾试验结果的判定方法，腐蚀物出现判定法：定性判定，试验后功能测试应 OK，外观观察产品无腐蚀现象产生。	目视/测试架/客户样机/显微镜
8	ESD 抗静电试验	测试架测试状态下试验：接触 4KV,非接触(空气) 8KV 放电测试	抗静电枪（尖头接触放电，圆头空气放电）	检验外观、功能	目视/测试架

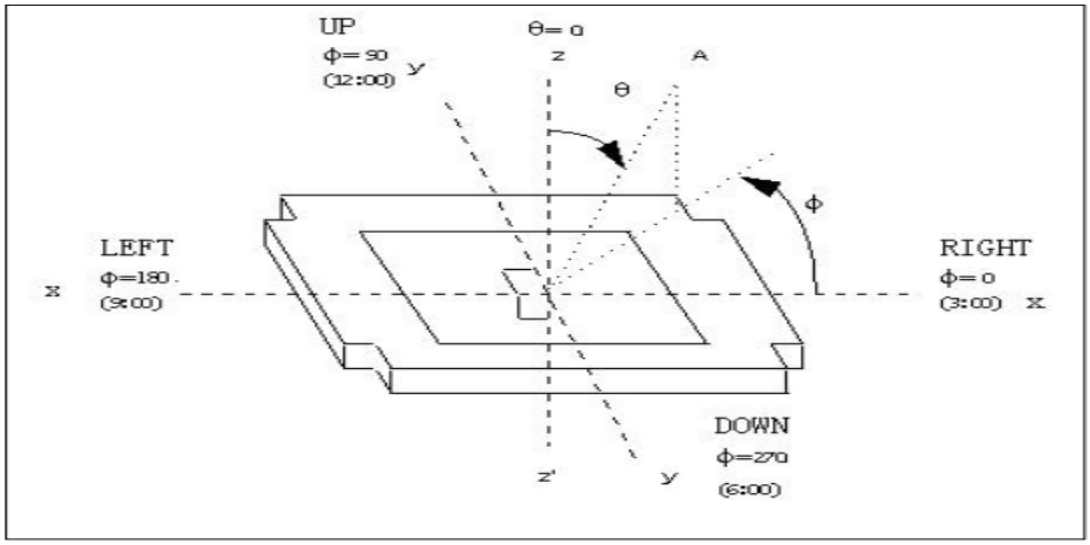
6. 光电参数（Optical Characteristics）

6-1. OPTICAL CHARACTERISTICS (LCD Panel+DrIC+STD_BLU)

LCD (BACKLIGHT ON)

Item		Symbol	Condition	Min	Typ	Max	Unit	Note
Transmittance		T	φ=0°, θ=0°	(3.23)	(3.85)	-	%	(1),(2),(7)
Viewing Angle		θ11	CR≥10	75	80	-	deg.	(3),(4),(5)
		θ12						
		θ21						
		θ22						
Contrast Ratio		CR	φ=0°, θ=0°	1100	1500	-	-	(1),(4)
Response Time		Tr+Tf	φ=0°, θ=0°	-	-	(25)	ms	(6)
		GtoG		-	-	(34)		
Chromaticity	Red	x	φ=0°, θ=0°	(0.631)	(0.646)	(0.661)	-	(2),(7)
		y		(0.327)	(0.337)	(0.347)		
	Green	x		(0.299)	(0.314)	(0.329)		
		y		(0.589)	(0.604)	(0.619)		
	Blue	x		(0.146)	(0.156)	(0.166)		
		y		(0.042)	(0.057)	(0.072)		
	White	x		(0.280)	(0.300)	(0.320)		
		y		(0.295)	(0.315)	(0.335)		
NTSC Ratio		-	φ=0°, θ=0°	(67)	(71)	-	%	(2),(7)
Flicker	60Hz			(-30)			dB	(8)
	45Hz			(-25)				

For details, refer to the Notes on the following pages.



7.检验标准（Inspection standard）

8.1 Inspection conditions is as follows

1) Viewing angle is within +-30° from vertical direction, as fig 1

2) Viewing angle is the angle defined in the drawing

3) Ambient temperature is approximately 25+-5° C

4) Ambient luminance is about 300~500 Lux.

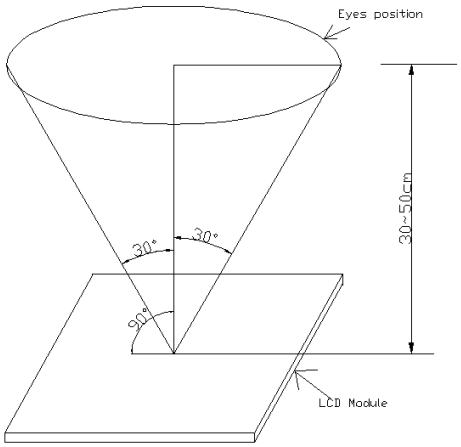
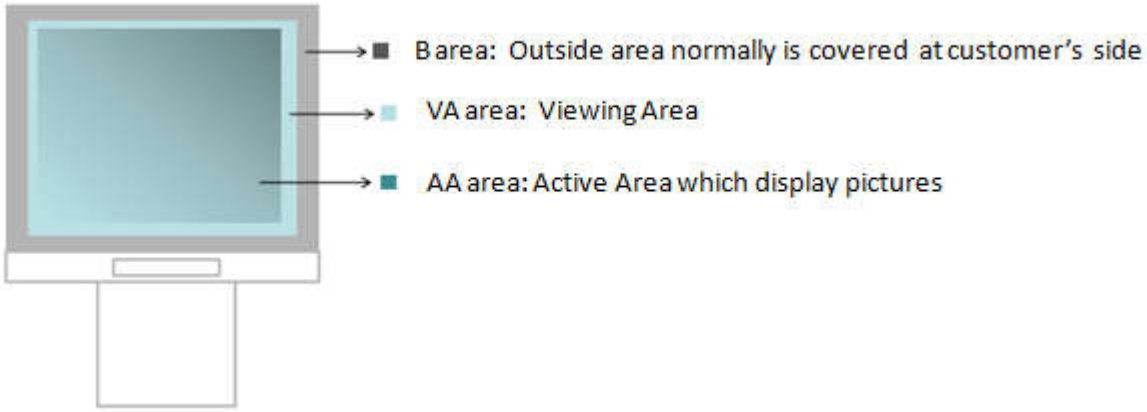
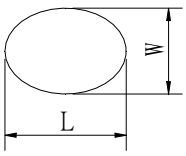


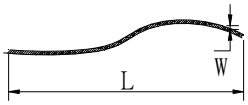
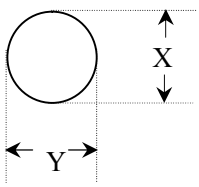
fig1

8.2 Panel area definition



8.3 Routine inspection standards

项目	不良定义	不良现象	判定标准			检验方法	
11.3.1	外观尺寸	与图纸尺寸不相符	NG			卡尺	
11.3.2	功能	显示少线	NG			目视	
		无显示	NG			目视	
		显示异常	NG			目视	主
		TP 功能不良，无触摸	NG			目视/用手触摸	主
11.3.3	*点亮产品可见及在LCD或T/P上有擦拭不掉的点状物*	*偏光片刺伤、脏点、圆形物、黑点*  *Φ=(L+W)/2*	LCM/总成 0.95 寸—2.4 寸			目视(用菲淋卡比对)	次
			Φ≦0.10mm		1、距产品30mm目视不见忽略。2、5mm间距内只允许3个点。3、显示区只允许10个点，超过以上第2第3项则NG 。		

<table>
<tr><td></td><td></td><td></td><td>0.10mm<Φ≦0.15mm</td><td></td><td>1</td><td></td><td></td></tr>
<tr><td></td><td></td><td></td><td>Φ>0.15mm</td><td></td><td>NG</td><td></td><td></td></tr>
<tr><td></td><td></td><td></td><td colspan="4">0.15mm<Φ≦0.2mm 按照 A-品入库</td></tr>
<tr><td></td><td></td><td></td><td colspan="3">LCM/总成>2.4 寸——6.0 寸</td><td rowspan="5">目 视
(用菲淋卡比对)</td><td rowspan="5"></td></tr>
<tr><td></td><td></td><td></td><td>Φ≦0.10mm</td><td></td><td>1、10mm 间距内只允许 3 个
2、显示区只允许 10 个点，超过以上任意一项则 NG</td></tr>
<tr><td></td><td></td><td></td><td>0.1mm<Φ≦0.15mm</td><td></td><td>4（TP、屏各允许 2 个）</td></tr>
<tr><td></td><td></td><td></td><td>0.15mm<Φ≦0.2mm</td><td></td><td>2（TP、屏各允许 1 个）</td></tr>
<tr><td></td><td></td><td></td><td>Φ>0.2mm</td><td></td><td>NG</td></tr>
<tr><td>11.3.4</td><td>点亮产品可见及在LCD或T/P上有擦拭不掉的线状物/刮伤</td><td>  </td><td colspan="3">LCM/总成 0.95 寸——6.0 寸
长(L) | 宽(W) | 允许个数
≦1mm | ≦0.03mm | 2
≦2mm | 0.03<W≦0.05mm | 1
>2mm | >0.05mm | NG
两条线毛之间必须距离 5mm 以上（0.95 寸—3.0 寸）.
两条线毛之间必须距离 10mm 以上（3.1 寸—6.0 寸）.</td><td>目视(用菲淋卡比对)</td><td>次</td></tr>
<tr><td>11.3.5</td><td>偏光片气泡</td><td>Φ=（X+Y）/2
  </td><td colspan="3">尺寸 | 允许个数
1、Φ≦0.1mm
2、不超过边框 1/3 | 不计(密集不可)
0.10<Φ≦0.2mm | 1
Φ>0.2mm | NG
0.2<Φ≦1.5mm,（边框以外） | 3
0.95 寸-2.4 寸气泡间距大于 5mm 以上
>2.4 寸-6.0 寸气泡间距大于 10mm 以</td><td>在日光台灯下撕起保护膜,距待测物 30cm 目视</td><td>次</td></tr>
</table>

			上		
11.3.6	T/P 及偏光片凹凸点	T/P：LCD 偏光片上有凹凸点	可视区有水纹（擦拭不掉）拒收 未进入可视区允收，客户装机后不见允收	在同一视角下用样品比对	次
11.3.7	Mura	边框四周或任一侧的色差、较画面深、区域云状不均、固定位置之图形凹陷状、封口部分较画面深的半圆形、一圈圈均匀的色差、线状 mura、黑画面可见因 spacer 聚集产生的 mura、均匀的实斜线、区域性斜线、Driver IC 与 TFT 匹配问题等原因的 mura	1.判定示画面为 128 灰阶画面，用 ND filter 盖住 mura 位置进行判定。 2、ND1.3（ND5%可遮盖不见） 3、双方若有签 限度样品，优先限度样品。	ND filter, 128 灰阶画面	次

8.模组使用注意事项（Precautions for Use of LCD Modules）

12.1 如果接口定义内有定义 IM0，请根据规格书（4.接口定义）内的定义做正确选择以匹配数据线的位数。

12.2 客户在做结构设计时，请保证机壳开窗尺寸比触摸屏 V.A 单边少 0.3mm。泡棉开窗尺寸比触摸屏 V.A 单边大 0.2mm。

12.3 模组的主要部件 LCD 和 TP 都是由玻璃组成，在测试、使用、移动过程中，请轻拿轻放。当产品不带触摸屏时，靠近 FPC 的屏幕两端绝对不能受力，否则会导致玻璃破损和显示不良的发生。

12.4 粘合偏光片、背光、触摸屏的胶材是有机物质，在接触到甲苯、乙醇、丙酮时，会破坏粘性。在使用中，请防止这些物质接触到产品。

12.5 如果显示表面掉落有灰尘、异物，切忌用手直接擦拭。请用棉签轻轻挑擦。

12.6 如果 LCD 破损导致液晶泄露，请不要让皮肤或衣服沾到液晶。如果不小心碰到，请立即用肥皂和清水清洗。

12.7 用手直接触摸显示区域会造成偏光片的损坏，同时容易引起静电问题。

12.8 当模组运行时，在显示区域施加压力会导致显示不正常。撤去外力，重新开机，可以恢复。

12.9 潮湿的坏境可能引起玻璃 ITO 的腐蚀，在使用中，请确保湿度在 50%一下。